REMARKS

This paper is filed in response to the Office Action mailed on April 20, 2004, and is therefore timely and Applicants respectfully submit that no extension of time fees are required. Further, only 2 independent claims and 16 claims in total are pending in this application and therefore no additional claim fees are required.

The specification is objected to due to a number of informalities and under 35 U.S.C. § 112, first paragraph. In response, the entire specification has been amended to traverse these objections. Similarly, all objections to the claims have also been addressed in the amendments to the claims.

Claims 1-4 stand rejected under 35 U.S.C. § 102(e) as being anticipated by "Ramkumar" (U.S. Patent No. 6,555,484).

As discussed in the specification as filed, the prior art teaches the use of ion implantation layers to control the threshold voltage in flash memory devices. However, the prior art ion implantation layers are formed by implanting boron or BF_2 in the p well. This process results in two problems. First, outgasing caused by the subsequent annealing process harms the oxide layer and, the use of high concentrations of boron result in TED (transient enhanced diffusion). Both of these problems can result in device failure.

Claims 1 and 9 both recite processes where a p well is first formed by implanting boron and then an ion implantation layer is formed by separately implanting a Group III monoatomic material into the p well layer at a predetermined depth to form an ion implantation layer. The ion implantation layer is then effectively used to control the threshold voltage. Further, by using a Group III monoatomic dopant having a molecular weight greater than boron, the inventors have found that outgasing and TED are minimized thereby resulting in improved device performance.

In contrast, Ramkumar does not teach or suggest the dual implantation technique recited in independent claims 1 and 9. Instead, Ramkumar only teaches a single implantation at column 3, lines 7-24 (see specifically line 15 where Ramkumar discusses "the implant").

Thus, Ramkumar does not teach or suggest forming a p well by first implanting boron into a semiconductor substrate to form a p well layer and then separately implanting a Group III monoatomic dopant into the p well layer to form an ion implantation layer within the p well layer. Accordingly, Ramkumar cannot serve

as an anticipating reference for independent claims 1 or 9 and the anticipation rejection is respectfully traversed.

Claims 5 and 6-8 stand rejected under 35 U.S.C. § 103 as being obvious in view of Ramkumar as combined with "Chen" (U.S. Patent No. 5,605,849) or Ramkumar in view of "Tsai" (U.S. Patent No. 6,245,639).

However, neither Chen nor Tsai teach or suggest that dual implantation within a p well layer of first creating the p well layer by implanting boron and then separately implanting a Group III monoatomic dopant having an atomic weight greater than boron to form an ion implantation layer within the p well layer for the purpose of controlling threshold voltage. Neither Chen or Tsai teach or suggest this means for preventing outgasing or TED which may occur during the subsequent annealing processes.

Accordingly, Applicants respectfully submit that the amendments to claims 1-8 traverse the obviousness rejections based upon Ramkumar and Chen or Ramkumar and Tsai.

Applicants also respectfully submit that new claims 9-16 are also allowable over the prior art of record.

An early action indicating the allowability of this application is respectfully requested.

The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855.

Respectfully submitted,

MARSHALL, GERSTEIN & BORUN LLP
6300 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606-6357
(312) 474-9577

July 20, 2004 By: _____

Michael R. Hull
Reg. No. 35,902